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Invention Name: Package Substrate

Invention Summary

Among the package substrate, IC chip side surface (above) of the weld pad is small (diameter 133 ~ 170 μ m), so weld metal pad for part of a relatively modest proportion. On the other hand, the surface of motherboard, etc. (below) of the welding pad large (600 μ m), a larger proportion of the metal parts. Here, the package substrate is, in the form of IC chips in the package substrate side, and used as a signal line conductor circuit 58U, 58U pattern between the temporary home 58M, to increase the package substrate side of the IC chip metal parts, In addition, the adjustment of the IC chip side and the motherboard side of the ratio of the metal parts, making the package substrate manufacturing process and the use does not produce deformities.

Invention

Technology

The present invention used to carry on a kind of IC chip package substrate, a more detailed words, there is about a difference above and below the formation of solder pads to connect IC chip (solder pad), and for connecting to the motherboard (mother board) and the second board (sub board) and other substrates of the package substrate solder pads.

High degree of IC chip set product loaded on the package substrate, and with the motherboard and the second board connected. Refer to Figure 23 to illustrate the packaging substrate structure, the figure shows the IC chip 80 loaded on the package substrate 600, and installed in the motherboard 90 of the state. Department of package substrate 600, the core substrate 630 on both sides of the formation of conductor circuits 658A, 658B; the conductor circuit 658A, 658B of the upper separated layer resin insulating layer 650 to form a conductor circuit 658C, 658D, and the conductor circuit 658C, 658D of the upper assembly the interlayer resin insulating layer 750. Moreover, interlayer resin insulating layer 650 to form interlayer hole 660B, 660A, and the interlayer resin insulating layer 750 to form interlayer hole 660D, 660C. On the other hand, rely on the surface of IC chip 80 (above) to form useful for connecting the IC chip 80 of the pad by welding projections 82, 676U, by the motherboard 90 of the surface (below) to form useful to rely on the motherboard to connect the pad 90 92 of the welding protrusions 676D. The welding protrusions formed in the solder pad 675U

676U, while the welding protrusions 676D 675D formed in the solder pads on. Here to improve the welding projections 676U and 676D of the connection reliability, so that IC chip package substrate 600 between 80 and 84 sealed with resin, the same, the package substrate 600 and the motherboard 90 to resin 94 between the seal with.

As mentioned above the package substrate 600 is used to connect IC chip 80 and the motherboard 90. That is, IC chip 80 of the pad 82 of the diameter of 133 ~ 170 μ m, while the motherboard 90 by the side of the pad 92 diameter 600 μ m, it can not be directly installed in the IC chip on the motherboard, it is interrupted package substrate conduct.

IC chip package substrate side solder pad 675U and motherboard side welding pad 675D, corresponding to the IC chip side of the pad 82 and the motherboard side of the pad 90 to form the size of 92. Therefore, the welding pad 675U in the package substrate 600 by IC chip side surface area proportion and the welding pad 675D motherboard in the side of the surface area occupied by different ratio. Here, the core substrate 630 to layer resin insulating layer 650 is formed using resin, while the welding pad 675U, 675D are formed by using nickel. Therefore, since the IC chip side surface by area proportion and the welding pad 675D motherboard in the side of the surface area occupied by the ratio of the difference between the manufacturing process, the interlayer resin insulating layer 650, 750 hardening, drying the resulting Some resin shrinkage, the package substrate to the IC chip side will bend. Moreover, when loading the actual use of IC chips, as part of the resin and metal parts welded pad shrinkage differences, IC chip due to thermal contraction and again will produce bending.

On the other hand, using multi-layer substrate as a package when the substrate, hence the plural layers including a layer conductor circuit as a ground layer conductor circuit or power supply level used to reduce the noise in order to achieve the purpose. However, as shown in Figure 23 technical multi-layer circuit boards known study is the ground layer by lines (or power level) to an external terminal. That is, the formation of the substrate 630 as a ground layer of the upper line 658A, 658B (conductor circuit). The line (ground line) 658B is mediated by the pore 660B and 658D-S connected to the line, and the line 658D-S is mediated by the pore 660D 675U connected with solder pads.

Here, the ground level 658D and 675U welding pad connection is via line 658D-S implementation, so line 658D-S susceptible to noise and the noise in the integrated set of chips for connecting the multi-layer circuit boards and other electronic devices malfunction because . Furthermore, we must empty out the line wound on the

multi-layer circuit board space, so will impede the conduct of high density.

On the other hand, in order to reduce IC chip and the motherboard signal between the noise, usually formed within the substrate in the package build appliances (condenser). 23 shown as an example, the core substrate 630 by setting both sides of the inner conductor circuit 658B, 658A to form a power layer and ground layer, to form the core substrate 630 exists in the storage of electrical appliances.

Figure 24 (A) is the formation of the core substrate 630 above the inner conductor circuit 658B of the view. The inner conductor circuit 658B form a ground layer 638G; and connect the upper and lower pad 640 with the ground. The ground pad 640 to form insulation around the buffer zone 642.

Ground pad 640 is shown through the first 23 of the core substrate 630 through the hole 636 of ground objects 640a; connected through the top of the layer of resin insulating layer 650 through holes 660A of the pad 640b; and the connection object 640a and the ground pad 640b of the line 640c posed.

Practice known among technology package substrate is grounded through line 640c to pad material 640a and 640b connected, so the upper and lower conductor layer of the transmission path between the conductor layer of a long and slow signals convey the same time, connect resistance change high.

Furthermore, as section 24 of the (A) shows, among the ground pad 640, line 640c and ground materials 640a and 640c and between the lines connected between the pad portion 640b corner K. In the package substrate thermal cycling process, the resin core substrate 630 and the interlayer resin insulating layer 650; with copper and other metal grounding pad 640 of thermal expansion different, so the stress will be concentrated in the corner of K, and as 23 chart as shown in the interlayer resin insulating layer 650 cracks L1, and so that the interlayer resin insulating layer 650 on the conductor circuit 658D or 660D mediated pore produce disconnected.

On the other hand, rely on the motherboard side of the weld projections 90 676D is mediated by the pore 660D-line 678 - soldering pad 675D and the inner conductor is connected to the circuit 658C. Article 24 (B) is an intermediary layer of Figure 23 holes 660D and 675D solder pad side view from the C state of enlargement. Load projections for welding the welding pad 675D 676D round, and through line 678 and form a circle as described above forming interlayer connection hole 660D.

Repeat the IC chip 80 for the high-temperature state in the action, while cooling to room temperature with the action end of the heat cycle. Here, the use of silicon chips form the IC package 80 and the resin substrate 600 made of the thermal expansion rate varies greatly, so in the course of the thermal cycle will produce stress in the package

substrate 600, package substrate 600 and the seal between the motherboard 90 94 resin cracks L2. Once the cracks of the resin 94 L2, L2, if the crack to expand it, package substrate 600 of the via hole and the soldering pad 675D 660D between the connection was cut off. That is, as Figure 24 (C), the display map of the intermediate layer 23 and solder pad hole 660D 675D direction from the D side view of the state to enlarge graph, which as cracking L2, made in connection with loading in the weld bulge welding pad material 676D 675D 660D and dielectric layer hole produced 678 broken lines.

To solve the above problems, this invention aims to provide a package substrate, which has a welding projections, without any bending.

The purpose of this invention is to provide a difficult subject to noise impact of the multi-layer circuit boards and multi-layer printed circuit board.

The purpose of this invention is to provide a package substrate, which can shorten the upper and lower conductor lines of the transmission path between conductor lines.

The purpose of this invention is to provide a package substrate, it does not produce solder pad and the via holes break between.

Invention reveals

Of claim 1 among the IC chip package substrate solder pad side of the small metal part of the welding pad proportion of small, motherboard and other large substrate side of the weld pad, so a larger percentage of metal parts. Here, the IC chip package substrate side of the conductor circuit pattern formed between the temporary home (dummy) pattern, to increase the metal parts, and adjust the motherboard side of the IC chip side and the ratio of the metal parts, it does not produce packaging substrate bending case. Above pattern is not a temporary home electrical appliance connected or build the value, only the value of a mechanical, so called pattern.

Of claim 2 among the IC chip package substrate solder pad side of the small metal part of the welding pad proportion of small, motherboard and other large substrate side of the weld pad, so a larger percentage of metal parts. Here, the IC chip package substrate side of the conductor circuit pattern formed around the temporary home outside the pattern, so as to increase the metal parts, and adjust the IC chip side and the motherboard side, while the proportion of the metal parts to improve the metal of the temporary home pattern of the Department, the Department of package substrate peripheral mechanical strength, and will not produce packaging substrate straightness.

Of claim 3 into the packaging substrate, will be supporting the outermost conductor circuit of the inner insulation layer of the lower layer conductor circuit as the power supply and / or ground layer, and the medium pore circuit directly connected to the conductor , and in the formation of interlayer pore welding projections, so the power

layer or ground layer and welding projections have no connections. Therefore, overlapping lines arising from the noise.

Of claim 4 into the packaging substrate, will be supporting the outermost conductor circuit layer 2 resin insulating layer between the lower assembly of the first two as a power conductor circuit layer and / or ground layer, and will refer directly connected pore 2 of conductor in the circuit, and in the formation of interlayer pore welding projections, so the power layer or ground layer and welding projections have no connections. Therefore, overlapping lines arising from the noise.

Of claim 5 and 6 into the packaging substrate, the grounding pad material and integration, and the ground between the object and the pad is not connected by lines, so the conductor can be shortened upper and lower layers of the conductor layer transmission path between the same time, reducing resistance. Furthermore, as the ground between the object and the pad without via connections, so the stress does not concentrate on line and grounding line and pad material and the connection between the Ministry and the package will create within the substrate caused by the stress concentration turtle crack led to the break.

Fan patent No. 7 among the packaging substrate, the welding projections formed in the interlayer hole, to make welding projections and medium pore can be directly connected, even if the package substrate of memory in the cracks, it will not In the welding protrusions and arise between the medium pore broken. That is, through the line will connect to solder lug and medium pore, and the welding protrusions carried on the package substrate solder pad, when once the cracks that exist within, to connect the via hole and the soldering pads of the circuit, will disconnected due to cracks generated. But, of claim 7 of the package substrate will not crack and break generated.

Of claim 8 into the packaging substrate, the welding projections formed in the interlayer hole, to make welding protrusions and holes can be directly connected coat, even if the package substrate of memory in the cracks, it will not In the welding protrusions and arise between the medium pore broken. Moreover, the welding projections formed in the pore complex into a medium, so even if a plurality of holes among the coat is not with such an internal connection, other medium pore can also be connected with the welding projections, so concrete to achieve phase stabilization. Moreover, the welding projections formed in a plurality of interlayer holes, can form a large hole for the via welding projections.

Moreover, the present invention can also be among the temporary home design and electrical power or ground plane to connect, or temporarily set design itself is power or ground layer. This prevents the noise signal.

Brief description of Schemata

Figure 1 shows the implementation of the present invention Cases 1 package substrate.

2 The picture shows the package 1 shown substrate X1-X1 transverse section.

Fig 3 ~ 9 photo shows the implementation of the present invention Cases 1 package substrate manufacturing process profile.

Figure 10 shows the implementation of the present invention 2 cases the packaging substrate.

Figure 11 (A) for the first two cases the package substrate to implement the view. And section 11 plan (B) for the IC chip to the bottom chart.

Figure 12 shows the IC chip 10 shown being carried on the package substrate, and the state installed in the motherboard.

Figure 13 shows the implementation of the present invention 3 cases of multi-layer printed circuit board of the profile.

Figure 14 shows the implementation of the present invention 3 cases of patients with multi-layer printed circuit board to change the profile.

15 Figure 4 shows the implementation of the present invention the packaging substrate profile cases.

Figure 16 (A) for the first 4 cases of copper in the implementation of the formation of the core substrate design view. Figure 16 (B) for the first 16 map (A) part of the enlargement.

Figure 17 shows the implementation of this invention 4 cases of patients with change package substrate profile.

Figure 18 (A) is formed in 4 cases of the implementation of changes to the packaging substrate patients conductor circuit view. Figure 18 (B) for the first 18 map (A) part of the enlargement.

Figure 19 shows the implementation of the present invention 5 cases of the package substrate profile.

Figure 20 shows the IC chip 19 shown being carried on the package substrate, and the state installed in the motherboard.

21 The picture shows the implementation of the present invention 5 cases the change package substrate profile cases.

21 Figure 22 The picture shows the X5-X5 of the transverse section.

23 The picture shows the most traditional technology package substrate profile.

Figure 24 (A) for the inner conductor 23 of the circuit diagram of the view. Figure 24 (B) for the first 23 charts see Figure C direction of the arrow. Figure 24 (C) D for the

first 23 charts viewing direction of the arrow diagram.

Better implementation of the forms of invention

(1 implementation of the cases)

Please refer to Figure 1, the implementation of the present invention Cases 1 package substrate structure. Figure 1 shows the profile of patients for the first implementation of the package substrate 1, the above is loaded with integrated circuit assembly (Figure not shown) of the state, and installed in the motherboard and constitute an integrated set of circuit package substrate. The package substrate has to set the circuit connected to the pad area of the welding projections 76U, and the pad for connection to the motherboard of the welding projections 76D, to achieve the transfer of the integrated circuit assembly - the signal between the motherboard and cut off from the motherboard power supply purposes.

Package substrate 30 above and below the core substrate to form the inner layer of copper as a ground pattern 34U, 34D. Furthermore, the inner layer copper pattern 34U of the upper separated layer resin insulating layer 50 to form a conductor circuit as a signal line and the temporary home design 58U 58M, and the formation of penetrating the interlayer resin insulating layer 50 of medium pore 60U. Conductor circuit 58U and 58M temporary home design across the upper layer resin insulating layer 150 to form the outer conductor circuit 158U and the penetration of the resin layer interlayer insulating layer 150, hole 160U. The outermost conductor circuit 158U and 160U mediated pore formation to support the welding projections useful to the welding pad 76U 75U. The diameter of solder pad 75U 133 ~ 170 μ m.

On the other hand, the core substrate 30 under the side of the ground layer (inner layer copper pattern) 34D of the upper separated layer resin insulating layer 50 to form the conductor circuit as a signal line 58D. Conductor circuit 58D of the upper separated layer resin insulating layer 150 to form the outer conductor circuit 158D and the penetration of the resin layer interlayer insulating layer 150, hole 160D. The outermost conductor circuit 158D and 160D mediated pore formation to support the welding projections useful to the welding pad 76D 75D. Soldering pad 75D motherboard side of the diameter of the form 600 μ m.

1 Figure X1-X1 of the section shown in Figure 2. That is, Figure 2 shows the cross section package substrate, and the No. 2 figure in the X1-X1 profile in the equivalent of 1 map. As shown in Figure 2, as the signal line of the conductor circuits 58U 58U-conductor circuit formed between a temporary home design 58M. Purchase patterns here are not a temporary electrical connection, or build the value of electrical appliances and so on, only a mechanical value, so called pattern.

23 Figure study with known technology as described in the first one embodiment of the package substrate, because each IC chip side surface of the solder pad assembly of small (diameter 133 ~ 170 μ m), so welding the portion of metal pad small proportion. On the other hand, due to the surface of the motherboard (below) of the welding pad large (diameter 600 μ m), so weld pad large proportion of the metal parts. The embodiment of the package substrate side by the IC chip as the signal line conductor circuit 58U, 58U pattern between the temporary home 58M, in order to increase the IC chip package substrate side of the metal parts, and adjust the package substrate of the IC chip side with the motherboard side of the ratio of the metal parts, making the latter package substrate manufacturing process, and not to bend in use.

Then give a specific example illustrates the package 1 shown substrate manufacturing method. First, note A. electrolytic plating with non-adhesive; B. interlayer resin insulating agent; C. resin filler; D. Welding photoresist composition.

A. Non-electrolytic gold plating materials used with the adhesive composition modulation (top with adhesive)

[Resin composition]

Ministry to take 35 to 25% of the weight of cresol novolac epoxy resin (Japan-based pharmaceutical manufacturer, molecular weight 2500) of allyl compounds to 80wt% concentration of resin solution dissolved in DMDG; 3.15 weight Department of photosensitive monomer (synthesis of East Asia system, ARONIX M315); 0.5 weight Department of defoamer (SAMNOPUKO system, S-65); and 3.6 weight of NMP to the Department of mixing derived.

[Resin composition]

The 12 weight polyether Department of sulfur (PES); 7.2 weight Department of epoxy resin particle (Sanyo Kasei system, POLYMERPOLE), while the average size of 1.0 μ m persons; 3.09 weight average particle size of the Department were mixed with 0.5 μ m , the Department added 30 weight NMP, using beads bubble mixer (beads mixer) for mixing.

[Hardening composition ®]

2 Department of taking the weight of imidazole hardening agent (Shikoku Chemical Manufacturing, 2E4MZ-CN); 2 the weight of the Department of photoinitiator (CIBA GEIGY IRUGAKYUA I-907); 0.2 Department of the light weight of sensitizer (Japan-based pharmaceutical manufacturer, DETX-S); and 1.5 weight NMP Department of mixing.

B. Modulation of interlayer resin insulating agent composition of raw materials used (lower with adhesive)

[Resin composition]

Ministry to take 35 to 25% of the weight of cresol novolac epoxy resin (Japan-based pharmaceutical manufacturer, molecular weight 2500) of allyl compounds to 80wt% concentration of resin solution dissolved in DMDG; 4 weight Department of photosensitive monomer (synthesis of East Asia system, ARONIX M315); 0.5 weight Department of defoamer (SAMNOPUKO system, S-65); and 3.6 weight of NMP to the Department of mixing derived.

[Resin composition]

The 12 weight polyether Department of sulfur (PES); 14.49 weight Department of epoxy resin particle (Sanyo Kasei system, POLYMERPOLE) average size of 0.5 μ m were mixed, add 30 weight Department of NMP, using beads bubble mixer (beads mixer) for mixing.

[Hardening composition ®]

2 Department of taking the weight of imidazole hardening agent (Shikoku Chemical Manufacturing, 2E4MZ-CN); 2 the weight of the Department of photoinitiator (CIBA GEIGY IRUGAKYUA I-907); 0.2 Department of the light weight of sensitizer (Japan-based pharmaceutical manufacturer, DETX-S); and 1.5 weight of NMP to the Department of mixing.

C. resin used filler material composition modulation

[Resin composition]

Part of 100 weight of bisphenol-type epoxy monomer (oil-based manufacturer of snow land, molecular weight 310, YL983U); 170 weight Department of silane coated with adhesives of the average size of 1.6 μ m of SiO 2 spherical particles (ADOMATEC manufacturing, CRS 1101-CE of its small particle size of the largest of the latter the thickness of the inner layer copper pattern); 1.5 weight Department of leveling agent (SAMNOPUKO manufacturing, PELENOLE S4) for mixing, so that the mixture adjusted to 23 ± 1 °C The viscosity of 45000 ~ 49000cps.

[Hardening composition]

6.5 weight Department of imidazole hardening agent (Shikoku Chemical Manufacturing, 2E4MZ-CN).

D. Welding photoresist composition

Mixing 46.67g of photosensitive oligomer (molecular weight 4000), which was dissolved in DMDG to 60 weight% of cresol novolac epoxy resin (Japan-based drug manufacturing) 50% of the proceeds of epoxy propylene; 15.0g of 80 weight% dissolved in methyl ethyl ketone of bisphenol A resin (oil-based snow land manufacturing, EPICOTE 1001); 1.6g imidazole hardening agent (Shikoku Chemical Manufacturing,

2E4MZ-CN); 3g of photosensitive monomer polyvalent acrylic monomer (Japan-based pharmaceutical manufacturer, R604); 1.5g many price propylene monomer (co-prosperity of chemical manufacturing companies, DPE6A); 0.71g of the dispersion of the antifoaming agent (SAMNOPUKO manufacturing, S-65) Moreover, addition of 2g in the mixture as a photoinitiator of diphenyl acetone (Kanto Chemical Manufacturing); and 0.2g as a light sensitizer Michler ketone (Kanto Chemical Manufacturing) to adjust its viscosity degree at 25 °C for the 2.0Pa · s, which are welded photoresist composition.

Furthermore, the use of B-type viscometer (Tokyo keiki, DVL-B type) for viscosity measurement, and 60rpm using rotor No.4, while 6rpm use rotor No.3.

Then, please refer to Figure 3, Figure ~ 9, which shows the manufacturing method of packaging substrate 100.

E. package substrate manufacturing

(1) the thickness of 1mm epoxy resin or BT (bismaleimide acid amide alkylamine triazine) resin as the substrate 30 on both sides of the stack (laminate) 18 μ m of copper foil 32 to form with copper laminates 30A, and 30A of the above copper laminate as starting materials (refer to Figure 3, the steps (A)). First, the copper laminate 30A drilling deal, and then to impose non-electrolytic plating, and the use of etching to form patterns on both sides of the substrate 30, forming the inner layer of copper 34U, 34D and 36 through the hole (Fig 3 of the steps (B)).

(2) to form the inner layer copper 34U, 34D and 36 of the substrate through holes 30 for washing, drying, by using NaOH (10g / l), NaClO 2 (40g / l), Na 3 PO 4 (6g / l) as oxidation bath, and use NaOH (10g / l), NaBH 4 (6g / l) as reduction bath to carry out the oxidation and reduction treatment to the inner copper 34U, 34D and 36 of through holes formed on the surface rough layer 38 (refer to Figure 3, the steps (C)).

(3) C of the resin used filler material composition modulation with hybrid mixing to get the resin filler.

(4) the use of spin coating machine will be prepared within 24 hours of the resin filler 40 coated on both sides of the substrate 30, to fill in the conductor circuit (inner layer copper pattern) 34U 34U and the conductor between the circuit and through the hole 36 in, and then dried at 70 °C for 20 minutes, on the other hand the same way the resin filler 40 filled in the conductor circuit 34D or through hole 36, the heat and drying at 70 °C for 20 minutes (see Fig 3 of the steps (D)).

(5) the use of belt sanding machine, and use the strip of abrasive paper # 600 (3 total management of chemical manufacturing), the above (4) deal with the completion of grinding one side of the substrate 30 until the inner layer copper pattern 34U, 34D surface and not through the hole 36 of the surface residual resin filler 40, and second, to

remove the belt sand to leave a light abrasive rubbing of injury. And also to the other side of a series of attrition treatment (refer to Figure 4 of the steps (E)).

Then, at 100 °C for 1 hour at 120 °C for 3 hours at 150 °C for 1 hour at 180 °C for 7 hours of heat treatment to harden the resin filler 40.

Were treated as above can be removed by filling in the holes 36 through the resin filler 40 and the inner layer copper pattern surface Department 34U, 34D above armoring layer 38, Er Shi smooth on both sides of the substrate 30, to obtain resin conductor circuit 40 and the inner filler 34 between the rough side of layer 38 secured to the circuit substrate strength. That is, this step allows the surface of resin filler 40 and the inner surface of copper pattern 34 for the same plane.

(6) to form a conductor circuit 34U, 34D of the substrate 30 to achieve a slight alkaline degreasing and etching, followed by the use of palladium chloride solution and organic acid as the catalyst for processing, but it has the Pd, the contact media activated, the substrate 30 impregnated at 3.2 × 10 -2 mol / l of copper sulfate, 3.9 × 10 -3 mol / l of nickel sulfate, 5.4 × 10 -2 mol / l the wrong mixture, 3.3 × 10 -1 mol / l of sodium hypophosphite, 5.0 × 10 -1 mol / l of boric acid, 0.1g / l of surfactant (Nissin Chemical Industry Manufacturing, SURFIL 465) constituted by a pH = 9 among the non-electrolytic plating solution, After 1 minute dipping every 4 seconds using the vertical and horizontal ground vibration 1, and in the conductor circuits 34 and 36 of the grounding through holes formed on the surface material 36a Cu-Ni-Pd composition of coarse needle-like alloy cladding layer of layer 42 (refer to Figure 4 of the steps (F)).

Furthermore, in the presence of 0.1mol / l of tin boride fluoride, 1.0mol / l of thio-urea, temperature 35 °C, pH = 1.2 under the conditions of Cu-Sn substitution reaction to the rough surface layer thickness of 0.3 μ m of Sn layer (Figure not shown).

(7) resin insulating layer B of the modulation agent mixing with the raw material composition, and adjusted to obtain the viscosity 1.5Pa · s the interlayer resin insulating agent (lower use).

Second, A non-electrolytic plating adhesive composition prepared mixing with raw materials, and adjusted to obtain the viscosity 7Pa · s non-electrolytic plating adhesive solution (upper only).

(8) using spin coating machine of the above (7) prepared within 24 hours the viscosity 1.5Pa · s interlayer resin insulating agent (lower use) 44 coated on the above (6) of the substrate on both sides, then place in the horizontal 20 min, then dried at 60 °C (pre-baking) for 30 minutes, and secondly, the above (7) modulation of viscosity within 24 hours 7Pa · s the photosensitive adhesive solution (top with) 46 coating on the substrate on both sides and then placed in the horizontal for 20 minutes, then dried at

60 °C (pre-baking) for 30 minutes, to form the thickness of 35 μ m of the adhesive layer 50 α (Please refer to Figure 4 of the steps (G)).

(9) to (8) form a layer of substrate adhesive seal printed on both sides of 30 with 85 μ m φ black circle of the mask membrane (Figure not shown), and then use high pressure mercury lamp with the intensity of 500mJ/cm 2 for exposure. Then spray DMTG solution for developing, re-use ultra high pressure mercury vapor lamps to 3000mJ/cm 2 of the intensity of exposure, and then at 100 °C for 1 hour, 120 °C for 1 hour, 150 °C for 3 hours of heat treatment (after baking) to form a film with a precise and equivalent to 85 μ m φ mask opening size (medium pore openings) 48, 35 μ m and the thickness of the interlayer resin insulating layer (layer 2 structures) 50 (please refer to section 5 charts Step (H)). Also, refer to the formation of pore opening 48 exposed part of the tin-plated layer (Figure not shown).

(10) 48 of the substrate to form openings 30 in 19 minutes soaking in chromic acid to remove dissolved present in the interlayer resin insulating layer of epoxy resin particles in the surface 50, to the layer of resin insulating layer between the rough surface 50 of (please refer to Figure 5 the steps (I)), after dipping in the middle and the solution (SPRAY, Inc) and then washed.

Furthermore, by processing in the rough (coarse depth of 6 μ m) imposed on the surface of the substrate after the palladium catalyst (ATOTEX manufacturing) process, to the interlayer resin insulating layer 50 and the opening 48 the inner wall surface of the formation of catalytic core .

(11) will be shown in the following composition impregnated substrate of non-electrolytic copper plating solution, the formation of all rough thickness of 0.6 μ m of non-electrolytic copper plated film 52 (refer to Figure 5 the steps (J)).

[Non-electrolytic plating solution]

EDTA 150 g / l

Copper sulfate 20 g / l

HCHO 30 ml / l

NaOH 40 g / l

α, α '- United 2 · Ding 80 mg / l

PEG 0.1 g / l

[Non-electrolytic plating conditions]

Liquid temperature of 70 °C for 30 minutes

(12) above (11) forming a non-electrolytic copper plating film 52 of the substrate paste commercially available photosensitive dry film, and then loading screen cover, and to 100J/cm 2 of the intensity of exposure, and then to 0.8% of sodium carbonate to

developing, to form a thickness of 15 μ m of gold-plated resist 54 (see Figure 6 of the steps (K)).

(13) Then, form a photoresist without some use of electrolytic copper plating to impose the following conditions to form a thickness of 15 μ m of the electrolytic copper plated film 56 (refer to Figure 6 of the steps (L)).

[Electrolytic plating solution]

Sulfuric acid 180 g / l

Copper sulfate 80 g / l

Additives (ATOTEX JAPAN manufacturing KAPARASIDO GL) 1 ml / l

[Electrolytic plating conditions]

Current density 1A/dm 2

Time 30 minutes

Temperature Room temperature

(14) using 5% KOH to strip plating resist 54, and then using sulfuric acid and hydrogen peroxide mixture for etching to remove the gold plating solution under the non-electrolytic copper plating resist film 52, to form non-electrolytic copper gold-plated electrolytic copper plating film 52 and 56 constitute a membrane thickness of 18 μ m of the conductor circuits 58U, 58D, and the medium pore 60U, 60D (6 diagram of steps (M)).

(15) for and (6) the same treatment, so that conductor circuits 58U, 58D and medium pore 60U, 60D of the surface of the Cu-Pd-Ni composition of the coarse surface 62, and then its surface Sn replacement (see section 7 Figure of steps (N)).

(16) repeat the above (7) ~ (15) steps to form the top of the conductor circuit. That is, using spin coater on both sides of the substrate 30, resin insulating layer coating agent (lower use), to form the insulator layer 144. Using spin coater on the insulator layer coated photosensitive adhesive 144 (top with), to form the adhesive layer 146 (refer to Figure 7 of the steps (O)). In the formation of insulator layer 144 and adhesive layer 146 of the substrate 30 on both sides sealed mask film, and then after exposure · develop to form with the opening (refer pore formation with the opening 148) of the interlayer resin insulating layer 150, after the interlayer resin insulating layer 150 into a rough surface (see Figure 7 of the steps (P)). After treatment in the rough surface of the substrate 30 formed on the surface of non-electrolytic copper plated film 152 (refer to Figure 8 of the steps (Q). Next, electrolytic copper plating film 152 in the non-set on gold after the photoresist 154, in the form of light is not blocking the formation of electrolytic copper plating film part 156 (refer to Figure 8 of Step (R)). Then, using gold-plated photoresist stripping 154 KOH, the solution to remove photoresist 154, the

following non-gold-plated electrolytic copper plating film 152, to form the conductor circuits 158U, 158D, and the medium pore 160U, 160D (See Figure 8 of the steps (S)). and then in the conductor circuit 158 and the via holes 160 formed on the surface armoring layer 162 (9th charts step (T)). However, the conductor circuit 158 formed in the pore and medium coarse surface layer 160 of 162 Sn without replacement.

(17) in the above (16) 30 on the substrate obtained by coating 45 μ m above described welding D. photoresist composition 70 α. Second, at 70 °C for 20 minutes at 70 °C for 30 minutes after drying, the thickness of 5mm and seal loading pattern depicted a circle (mask to pattern) of the mask membrane (Figure not shown), and to 1000J/cm 2 UV expose, and to DMTG for imaging processing. Then at 80 °C for 1 hour, 100 °C for 1 hour, 120 °C for 1 hour, 150 °C for 3 hours, heating, and welding pad portion (including the via hole and the ground material part) forming openings (opening diameter 20 μ m) 71 welding photoresist layer (thickness 20 μ m) 70 α (refer to Figure 9 the steps (U)).

(18) Second, the substrate 30 impregnated in 2.31 × 10 -1 mol / l of nickel chloride, 2.8 × 10 -1 mol / l of sodium hypophosphite, 1.85 × 10 -1 mol / l sodium form of lemon The pH = 4.5 the non-electrolytic nickel plating solution after 20 minutes, the openings 71 formed in the thickness of 5 μ m nickel plating layer 72. Furthermore, the substrate dipped in 4.1 × 10 -2 mol / l of gold potassium cyanide, 1.87 × 10 -1 mol / l of aluminum chloride, 1.16 × 10 -1 mol / l of sodium lemon, 1.7 × 10 - 1 mol / l sodium hypophosphite constitutes a non-electrolytic gold plating liquid in 7 minutes 20 seconds to form a nickel plating layer thickness of 0.03 μ m gold 74 K gold-plated layer, referred to in the pore 160U, 160D and the conductor circuit 158U, 158D form a welding pad 75U, 75D.

(19) Then, photoresist layer 70 in the welding openings 71, adhesive printing solder paste (paste), by re-heat at 200 °C (reflow) to form the welding projections (welding body) 76U, 76D, and the formation of package substrate 100 (see Figure 1).

Moreover, the implementation of the cases is the use of semi-additive method examples of the formation of packaging substrate, the structure of this invention can be applied to the whole course, the formation of additive package substrate.

1 implementation of the cases were formed in the interlayer resin insulating layer 50 and interlayer resin insulating layer 150 formed between the conductor circuit 58U temporary home design 58M, however, the core substrate to form the inner layer copper pattern 30 or the outer conductor 34D between the temporary circuit 158U 58M can buy patterns.

Described in paragraph 1 above cases the implementation of the packaging substrate, the substrate of the IC chip package as a signal line side of the conductor circuit pattern formed between the temporary home, an increase of the IC chip package

substrate side of the metal parts, and adjust the IC chip side with the motherboard side of the ratio of the metal parts, so too in the package substrate in the manufacture and use will not produce bending.

(2 implementation of the cases)

Please refer to Figure 10 to 12 to illustrate the implementation of the present invention 2 cases. 10 Figure 2 shows the implementation case of the package substrate profile. Figure 11 (A) shows the top view package substrate, while Figure 11 (B) shows the IC chip 80 are packed in 10 packages shown above, the state of the substrate, and installed in the motherboard 90 of the state profiles. As shown in Figure 12, above the package substrate with IC chips to connect the pad 80 of the welding projections 82 76U, and in the following to connect the motherboard 90, with 92 of the welding pad projections 76D, in order to achieve transfer of the product set circuit - the signal between the motherboard and power supply cut off from the purpose of the motherboard.

As shown in Figure 10, package substrate 30 above and below the core substrate to form the inner layer as a ground layer copper pattern 34U, 34D. Furthermore, the inner layer copper pattern 34U of the upper separated layer resin insulating layer 50 to form the circuit as a signal line conductor 58U, and the formation of penetrating the interlayer resin insulating layer 50 of medium pore 60U. Conductor circuit 58U across the upper layer resin insulating layer 150 to form the outer layer conductor circuits 158U, 159 and the temporary home design through the resin layer interlayer insulating layer 150, hole 160U. As shown in Figure 11, the temporary home design 159 formed in the peripheral conductor circuits 158U, that is, along the margin of the Department of package substrate formation. Conductor circuit 158U and 160U mediated pore formation helpful to support the solder pad welding protrusions 76U 75U. The IC chip side solder pad 75U diameter of 123 ~ 170 μ m.

On the other hand, the core substrate 30 under the side of the ground layer (inner layer copper pattern) 34D of the upper separated layer resin insulating layer 50 to form the conductor circuit as a signal line 58D. Conductor circuit 58D of the upper separated layer resin insulating layer 150 to form the outer conductor circuit 158D and the penetration of the resin layer interlayer insulating layer 150, hole 160D. The conductor circuit 158D and 160D mediated pore formation to support the welding projections useful for welding pad 76D 75D. Soldering pad 75D motherboard side of the diameter of the form 600 ~ 700 μ m.

Figure 11 (A) for the package substrate 200 of the view. That is, for the first 10 A map of the view direction of the arrow diagram. 10 Figure 11 Figure is equivalent to

(A) vertical section of the X2-X2. Such as Figure 11 (A) and 10 as shown, as the signal lines around the outer conductor circuit 158U, and forms a temporary home design 10mm size 159, which was formed in the solder resist layer and the lower 70. Purchase patterns here are not a temporary electrical connection, or build the value of electrical appliances and so on, only a mechanical value, so called pattern.

23 Figure study with known technology as described in the first one embodiment of the package substrate, because each IC chip side surface of the solder pad assembly of small (diameter 120 ~ 170 μ m), so welding the portion of metal pad small proportion. On the other hand, due to the surface of the motherboard (below) of the welding pad large (diameter 600 ~ 700 μ m), so weld pad large proportion of the metal parts. The embodiment of the package substrate by the IC Chip side of the outer conductor circuit 158U Temporary home of peripheral pattern formation 159 To increase the package substrate IC Metal parts of the chip side, and adjust the package substrate IC Chip side and the proportion of the metal parts of the motherboard side, while the temporary home by metal pattern 159 To improve the package substrate mechanical strength margin of the Department, making the latter package substrate manufacturing process, and not to bend in use.

Complete view of the packaging substrate (S 10 Charts A View Map direction of the arrow) Shown in the first 11 Map (A) And section 11 Map (B) Show IC Chip bottom graph. In IC Chip 80 Loaded in the package substrate 200 State heat flow through the furnace again, as the first 12 Shown below, can be used welding projections 76U The IC Chip installed. After the assembly has IC Chip package substrate 200 Load on the motherboard 90 On, and then through the heat furnace to carry out the package substrate 200 On the motherboard 90 Installation.

Please refer to section 3 Map ~ S 9 Diagram to illustrate the above 2 Implementation cases ~ The latter section 5 Implementation of the case of package substrate manufacturing method, because methods with the first 1 Implementation of the cases of the same, so their description is omitted.

Furthermore, the above 2 Implementation of the cases in the interlayer resin insulating layer 150 The outermost layer of the upper layer conductor circuit 158U Formed around the outer temporary home design 159 However, in the formation of the core substrate 30 The inner copper pattern 34D Or the interlayer resin insulating layer 50 · Interlayer resin insulating layer 150 Between the conductor circuit 58U Pattern around the formation of temporary home 159 Also.

Described in the above paragraph 2 Implementation of the case of the packaging

substrate, the package substrate IC Chip side of the outer conductor circuit pattern formed around the temporary home, an increase of package substrate IC Metal parts of the chip side, and adjust the IC Chip side and the proportion of the metal parts of the motherboard side, so too in the manufacture of packaging substrate and the use will not produce bending.

(S 3 Implementation cases)

Please refer to section 13 Figure to illustrate the invention of the first 3 Implementation of the case of package substrate.

Package Substrate 300 The core substrate 30 The top of the formation as a signal line (Inner layer copper pattern) 34U , And the following line to form the inner layer of copper as the signal pattern 34D . Furthermore, the inner copper pattern 34U Across the upper layer resin insulating layer 50 Forming a conductor circuit as a signal line 58U . Conductor circuit 58U Across the upper layer resin insulating layer 150 Formation of the outermost conductor circuit 158U And penetrate the interlayer resin insulating layer 150 Dielectric layer hole 160U . The coat hole 160U Forming a welding projections 76U . That is, the first 3 Implementation of the cases were installed in the composition layer conductor circuit power 58U The medium pore 160U Projections on the formation of welding 76U Can be directly connected to the external projections (Figure not shown) .

On the other hand, the core substrate 30 The following line as a signal (Inner layer copper pattern) 34D Across the upper layer resin insulating layer 50 Forming a conductor circuit as a signal line 58D . Conductor circuit 58D Across the upper layer resin insulating layer 150 Formation of the outermost conductor circuit 158D And penetrate the interlayer resin insulating layer 150 Dielectric layer hole 160D . The coat hole 160D Forming a welding projections 76D . That is, the implementation of the cases were installed in the ground layer conductor circuit form 58D The medium pore 160D Projections on the formation of welding 76D Can be directly connected to the external projections (Figure not shown) .

The structure for the implementation of cases will be used to support the assembly in the outer conductor circuit 158U , 158D The interlayer resin insulating layer 150 The lower side of the conductor circuit 58U , 58D As the power layer and ground layer, and the medium pore 160U , 160D Directly connected to the conductor circuit 58U , 58D And the welding projections 76U , 76D The hole formed in the interlayer, so the power layer and ground layer and the welding protrusions have no connections. Therefore, because of line overlap from the impact of noise can reduce the active set of circuit · The signal transfer between motherboard

and power supply cut off from the motherboard when the noise effect. Moreover, the wireless way, it can reach a high density multi-layer printed circuit board purposes. Moreover, the multi-layer printed circuit board in this embodiment being, although the conductor circuit, respectively 58U As the power layer, the conductor circuit 58D As a ground layer, but in combination, the same floor with the power supply circuit conductor layer functions and functions with the ground conductor circuit layer to form a conductor circuit 58U Or the conductor circuit 58D Can.

Then, please refer to section 14 Figure to illustrate the first 3 Implementation of the cases of change cases, the Department of multilayer printed circuit board on.

S 14 Figure shows the first 2 Multi-layer printed circuit board embodiment of the construction section. The core substrate 230 The above and below ground level as the formation of the inner layer copper pattern 234U , 234D . That is, across the board 230 Corresponds to the ground floor with (Inner layer copper pattern) 234U And the ground floor (Inner layer copper pattern) 234D To form an electrical store.

Inner layer copper pattern 234U Across the upper layer resin insulating layer 250 Forming a conductor circuit as a signal line 258U . Conductor circuit 258U Across the upper layer resin insulating layer 350 Through the formation of interlayer resin insulating layer 350 Dielectric layer hole 360U . The coat hole 360U Forming a welding projections 376U .

On the other hand, substrate 230 Below ground level (Inner layer copper pattern) 234D Across the upper layer resin insulating layer 250 Forming a conductor circuit as a signal line 258D . Conductor circuit 258D Across the upper layer resin insulating layer 350 Forming a conductor layer as power supply circuit 388D . Conductor circuit 388D Penetrating the upper layer forming resin insulating layer 390 Dielectric layer hole 380D , And the medium pore 380D Forming a welding projections 376D

That is, the implementation of the cases were installed in the conductor layer as power supply circuit 388D Dielectric layer hole 380D Forming a welding projections 376D And external projections (Figure not shown) Can be directly connected with the power level.

S 3 Embodiment of the structure to change cases, the conductor layer as power supply circuit 388D And medium pore 380D Directly connected, and that the pore formation mediated welding projections 376D , So the power level and the welding protrusions have no connections. Therefore, without the noise due to the impact of line overlap.

Section described above 3 Implementation of the package substrate among patients, will be formed in supporting the outermost layer of the lower conductor circuit of the inner conductor insulation as the power circuit layer and / Or ground plane, and the via holes connect directly to the section 2 Conductor circuit, the medium pore forming welding projections, so the power level or ground level and there is no line between the welding lug connected. Therefore, the noise from the impact of line overlap. Moreover, the wireless way, it will bring high-density multi-layer circuit board of purpose.

Furthermore, the first 3 Implementation of the cases among the package substrate, will form the outer conductor in supporting the first circuit 2 Interlayer resin insulating layer side of the section under 2 Conductor circuit as the power level and / Or ground plane, and the via holes connect directly to the section 2 Conductor circuit, the medium pore forming welding projections, so the power level or ground level and there is no line between the welding lug connected. Therefore, the noise from the impact of line overlap. Moreover, the wireless way, it will bring high-density multi-layer circuit board of purpose.

(S 4 Implementation cases)

Please refer to section 15 Figure to illustrate the invention of the first 4 Embodiment of the packaging substrate structure. Package Substrate 400 The core substrate 30 Above and below ground level as the formation of the inner layer copper pattern 34U , 34D . Furthermore, the inner copper pattern 34U Across the upper layer resin insulating layer 50 Forming a conductor circuit as a signal line 58U And penetrate the interlayer resin insulating layer 50 Dielectric layer hole 60U . Conductor circuit 58U Across the upper layer resin insulating layer 150 Formation of the outermost conductor circuit 158U And penetrate the interlayer resin insulating layer 150 Dielectric layer hole 160U . The conductor circuit 158U And the medium pore 160U Helpful to support the formation of welding projections 76U Welding cushion 75U . This IC Chip solder pad 75U Diameter 133 ~ 170 μ m .

On the other hand, the core substrate 30 Lower side of the inner copper pattern 34D Across the upper layer resin insulating layer 50 Forming a conductor circuit as a signal line 58D . Conductor circuit 58D Across the upper layer resin insulating layer 150 Formation of the outermost conductor circuit 158D And penetrate the interlayer resin insulating layer 150 Dielectric layer hole 160D . The conductor circuit 158D And the medium pore 160D Helpful to support the formation of welding projections 76D Welding cushion 75D . Motherboard side

of the weld pad 75D The diameter of the form 600 μ m . Moreover, across the board 30 Set corresponds to the inner copper pattern 34U , 34D Ground floor assembly (Ground floor) And two inner copper 34U , 34D Can form an electrical store.

S 16 Map (A) In the core substrate 30 Above the inner layer copper pattern formation 34U Of the view. The inner copper pattern 34U Including, ground floor 34G ; And to connect the upper and lower grounding pads 41 . S 16 Map (B) Display section 16 Map (A) Map B Area ground pad 41 Enlarged map. S 16 Map (B) In X3-X3 Section corresponding to section 15 Charts X3-X3 Section.

If the first 16 Map (B) Shows, the ground pad 41 Order to make the first 15 Through the hole shown below 36 The ground material 41a , And for connecting to penetrate the upper layer of resin insulating layer 50 The medium pore 60U The pad 41b Into one person, and the grounding pad 41 Fitted around the size of about 200 μ m Insulating buffer zone 43 .

If the first 16 Map (B) Shown, this embodiment of the package substrate into, the ground material 41a And pad 41b Integration, and the ground material 41a And pad 41b No connection between the through line, so the lower (The core substrate 30 The lower conductor circuit 58D) And upper (Interlayer resin insulating layer 50) On the side of the conductor circuit 58U Shorten the path between the transmission and improve the signal transmission speed, while reducing resistance. Furthermore, the ground material 41a And pad 41b With connections between the need, not as the first 24 Map (A) Known technology as described in study, stress concentration on the line and ground line and the pad material as well as between the junction between the situation, therefore, does not produce the crack caused by stress concentration within the package substrate break. Here only for the core substrate 30 On the side of the inner copper pattern 34U For icon and description, but the lower side of the inner copper pattern 34D Also has the same structure.

Then, please refer to section 17 Map and section 18 Diagram to illustrate the first 4 Implementation of the case of the change cases. In the above 15 The first figure 4 Implementation of the cases among the substrates in the formation of the core 30 Both sides of the inner copper pattern 34U , 34D To form a ground layer (Electrode layer) 34G And the grounding pad 41 . Compared with this, the first 4 Change the case of patients being implemented in the form in the interlayer resin insulating layer 50 Top of the conductor circuit 58U , 58D On

the formation and first 16 Map (A) The same power level (Electrode layer) 58G And the grounding pad 61 .

S 17 The picture shows the first 4 Change the case of the implementation of Cases package substrate profile, and section 18 Map (A) Was formed in the interlayer resin insulating layer 50 Above the conductor circuit 58U Of the view. Conductor circuit 58U Forming a power level 58G And to connect the upper side and lower side of the grounding pad 61 . S 18 Map (B) Display section 18 Map (A) In B Grounding pad as shown in 61 Area enlargement. S 18 Map (B) S X4-X4 Cross-section corresponding to section 17 Shown below X4-X4 Section.

If the first 17 Shown, grounding pad 61 As, to make connections in the inner layer copper pattern 34U The through hole 60U Ground material 61a , And for connecting to penetrate the upper layer of resin insulating layer 150 The medium pore 160U The pad 61b Into one person, and as the first 18 Map (B) Shown, the grounding pad 61 Fitted around the outer dimensions of about 200 μ m Insulating buffer zone 63 .

S 4 Implementation of the cases among the packaging substrate, the ground material 61a And pad 61b Integration, and the ground material 61a And pad 61b No connection between the through line, so the lower (The core substrate 30 The top of the inner copper pattern 34U) And upper (Interlayer resin insulating layer 150) On the side of the conductor circuit 158U Shorten the path between the transmission and improve the signal transmission speed, while reducing resistance. Furthermore, the ground material 61a And pad 61b With connections between the need, not as the first 24 Map (A) Known technology as described in study, stress concentration on the line and ground line and the pad material as well as between the junction between the situation, therefore, does not produce the crack caused by stress concentration within the package substrate break.

Moreover, the implementation of the cases to a circular grounding pad material and integration, but the invention also allow the oval, polygonal and other shapes of earth materials and pad integration.

The description of the first 4 Implementation of the package substrate among patients, between the grounding pad material and do not need to connect through the line, so the lower and upper conductor lines (Conductor layer) Shorten the path between the transmission and improve the signal transmission speed, while reducing resistance. And because the ground between the material and the pads do not need to connect through the line, so not to stress concentration on the line and ground line and

the pad material as well as between the junction between the situation, therefore, does not produce the crack due to stress concentration disconnection caused by circumstances within the package substrate.

(S 5 Implementation cases)

Please refer to section 19 Map and section 20 Figure to illustrate the invention section 5 Embodiment of the package substrate. S 19 Figure shows the packaging substrate 500 For the first 20 Load have shown above IC Chip 80 State, and installed in the motherboard 90 The so-called integrated circuit package assembly substrate.

Package substrate core substrate 30 Above and below ground level as the formation of the inner layer copper pattern 34U , 34D . Furthermore, the inner copper pattern 34U Across the upper layer resin insulating layer 50 Forming a conductor circuit as a signal line 58U And the formation of resin through the layer of insulation between 50 Dielectric layer hole 60U . Conductor circuit 58U Across the upper layer resin insulating layer 150 Formation of the outermost conductor circuit 158U And penetrate the interlayer resin insulating layer 150 Dielectric layer hole 160U . The outermost conductor circuit 158U And the medium pore 160U Helpful to support the formation of welding projections 76U Welding cushion 75U . This IC Chip side of solder pad 75U Diameter 133 ~ 170 μ m .

On the other hand, the core substrate 30 Lower side of the ground plane (Inner layer copper pattern) 34D Across the upper layer resin insulating layer 50 Forming a conductor circuit as a signal line 58D . Conductor circuit 58D Across the upper layer resin insulating layer 150 Formation of the outermost conductor circuit 158D And penetrate the interlayer resin insulating layer 150 Dielectric layer hole 160D . The outermost conductor circuit 158D And the medium pore 160D Helpful to support the formation of welding projections 76D Welding cushion 75D . Motherboard side of the weld pad 75D The diameter of the form 600 μ m .

S 5 Implementation of the cases among the packaging substrate, by the motherboard 90 The welding projections 76D The formation of interlayer pore 160D Therefore, welding projections and medium pore can be directly connected, so even if the package substrate has cracks in the welding projections 76D And medium pore 160D Not arise between the break. That is, the light of article 24 Map (B) Shows, the most traditional technique is via the line 678 The welding pad 675D Connected to the medium pore 660D And the welding projections 676D Loaded in

the welding pad 675D The package substrate 600 In-house cracks L2 When, because of cracks L2 Made to connect the via hole 660D And welding pad 675D Line between 678 Break, and cut off the welding projections 676D And medium pore 660D . Compared with this, the first 5 Implementation of the case of the packaging substrate even if there is cracking and has no welding projections 76D And medium pore 160D Break between.

Then, for IC Chip 80 Installed in the first 19 The section shown 5 Implementation of the package substrate cases 500 Illustration. If the first 20 Shown below, will IC Chip 80 Corresponds to the IC Chip solder pad 82 To load the package substrate 500 The welding projections 76U , By examining the package substrate through the furnace to weld projections 76U Melting at IC Chip 80 The welding pad 82 On the package substrate to make 500 And IC Chip 80 Connection.

Then, using heat to purify the weld projections 76U Melting and solidification in the weld pad 82 When welding agent (Flux) . At this point, chlorine Sen (Chlorothen) Inflow of other organic solvents IC Chip 80 And package substrate 500 Between the gap in order to remove the solder. Then, the resin filled in IC Chip 80 And package substrate 500 Between, for resin sealing. Although the map does not appear, however, at the same time by modeling the resin completely (Molding) In IC Chip 80 , And the completion IC Chip 80 Installation.

Then, the package substrate 500 Installed on the motherboard 90 On. And package substrate 500 Welding projections 76D Corresponds to the welding pad motherboard 92 Load, through the package substrate through the furnace to weld projections 76D Melting in the motherboard 90 The welding pad 92 On the package substrate to make 500 And motherboard 90 Connection. If, after the first 20 Shown below, the resin 94 Fill in the package substrate 500 And motherboard 90 Between, for resin sealing, and complete the installation.

Then, please refer to section 20 Map and section 21 Figure, which shows the invention of the first 5 Change the case of the implementation of the package substrate cases 501 .

Please refer to section 19 Figure, above 5 Implementation of the package substrate Cases 500 Among the 1 A welding projections 76D Loaded in 1 A medium pore 160D . Compared with this, please refer to section 21 Figure, the first 5 Implementation of the package substrate Cases 501 Among the 1 A welding projections 276 Loaded in a plurality of (3 A) Coat hole 260,260,260 . That is, the first 21 As shown in Figure X5-X5 Line is equivalent

to the first 22 Map (S 22 Charts X6-X6 Line is equivalent to the first 21 Charts X5-X5 Line) , Which makes 3 A medium pore 260 Close, and the nickel-plated layer 72 And gold plating layer 74 The hole formed in the interlayer 260 Ministry of ground objects 260a , To form 1 Large earth materials 275 . Then the projections of large welded 276 Material loaded on the large ground 275 On.

Above 5 Change the case of the implementation case of the package substrate 501 Among the welding projections 276 Hole formed in the interlayer 260 On the projections to enable welding 276 And medium pore 260 Direct connection, so even if package substrate 501 There is cracking, do not cause welding projections 276 And medium pore 260 Arise between disconnected. Moreover, welding projections 276 Dielectric layers formed in a plurality of holes 260,260,260 Even if a plurality of holes into the interlayer 1 Not with the inner layer of a conductor circuit 58D Connection, the other medium pore of the Department, also welding projections 276 And the inner conductor circuit 58D Connection, it can achieve phase stabilization of specific (Phase safe) .

Furthermore, as mentioned above, IC Chip 80 Side of the weld pad 75U The diameter of 133 ~ 170 μ m , While the motherboard side of the weld pad 75D Diameter 600 μ m Both have 4 ~ 5 Fold difference, it is difficult in the motherboard side of the formation of large welded pad 75D In 1 A medium layer hole. Therefore, the first 5 Change the case of the implementation case of the package substrate 501 Among the projections by the welding 276 Formed in a medium pore complex 260,260,260 On the formation of large-scale welding projections. Among patients with these changes, although 3 A medium layer to form holes 1 A welding projections, however, can also 2 A medium layer to form holes 1 A welding projections Moreover, they can 4 A medium layer to form holes 1 A welding projections.

The description of the first 5 Implementation of the cases among the packaging substrate, through the projections in the welding hole formed in the interlayer, so that welding projections and medium pore can be directly connected, even if the package substrate, cracking into existence, and has no welding projections between the holes and broken coat. Furthermore, because the welding protrusions formed in a plurality of interlayer hole, so even if a plurality of holes into coat 1 Were not with the internal connection, other medium pore can also be connected with solder lug, and specifically the implementation phase can be stabilized. And, because welding projections formed in a plurality of interlayer hole, so we can form a large hole for interlayer welding

projections.

Among the above-mentioned embodiment, although the example of a direct connection to the mother board packaging board, but the packaging substrate of this invention is also applicable to the package substrate through the second plate connected to the motherboard of the situation.

Claims:

1. A kind of package substrate, the substrate on both sides across the core layer resin insulating layer forming a conductor circuit, and can be loaded in IC Chip-side solder pads are formed on the surface, and can be connected to other side of the surface of the substrate to form than the above IC Chip-side solder pads are relatively large load of the welding pad, characterized in that:

In the formation of the core substrate can be loaded in the IC Chip side of the conductor circuit pattern formed between the temporary home design.

2. A kind of package substrate, the substrate on both sides across the core layer resin insulating layer forming a conductor circuit, and can be loaded in IC Chip-side solder pads are formed on the surface, and can be connected to other side of the surface of the substrate to form than the above IC Chip-side solder pads are relatively large load of the welding pad, characterized in that:

In the formation of the core substrate can be loaded in the IC Chip side of the conductor circuit pattern formed around the temporary home outside the pattern.

3. A kind of package substrate, with most of its outer conductor for the circuit; support of the outermost conductor circuit of the insulating layer; and the insulating layer at the lower side of the inner conductor of the multi-layer circuit board, characterized in that:

The inner layer and conductor circuit for power / Or ground level, and through the insulation layer and connecting the inner conductor circuits formed on the via hole with a welding projections.

4. A kind of package substrate, which is equipped with the first 1 Inner conductor circuit; formed in the first 1 Layer above the first conductor circuit 1 Interlayer resin insulating layer; formed in the first 1 Interlayer resin insulating layer at the top of the first 2 Inner conductor circuit; formation of the section of the 2 The top of the first inner conductor circuit 2 Interlayer resin insulating layer; and formed in the first 2 Interlayer resin insulating layer at the top of the outer circuit of the multi-layer printed circuit board conductors, characterized in that:

Above 2 Inner conductor for the power circuit layer and / Or ground level, and through the first 2 Interlayer resin insulating layer and the connection of the first

2 Inner conductor circuits formed on the via hole with a welding projections.

5. A kind of package substrate, on both sides of the core substrate to form a conductor layer, and then across the interlayer resin insulating layer formed of another conductive layer, the core substrate layer on either side of the conductor as the electrode layer, characterized in that:

The assembly as the electrode layer on the conductor layer through use of the core substrate material through the holes of the ground; and to connect through the top of the layer interlayer resin insulating layer of the pad hole integration.

6. A kind of package substrate, on both sides of the core substrate to form a conductor layer, and then across the interlayer resin insulating layer formed of another conductive layer, any of the above interlayer resin insulating layer above the conductor layer can be used as an electrode layer, characterized in that:

The assembly as the electrode layer on the conductor layer below the layer resin insulating layer through holes in the ground with a coat material; and to connect through the layer above the interlayer resin insulating layer hole of the pad integration.

7. A kind of package substrate, separated by a plurality of interlayer resin insulating layer to form the multi-conductor circuit, and can be loaded IC Chip side surface, and can connect other side of the surface of the substrate to form welding projections, and in the substrate can be connected to the other side of the substrate surface and the other was between the resin sealing, characterized in that:

Will have access to the other side of the substrate surface welding protrusions formed in the via hole.

8. A kind of package substrate, separated by a plurality of interlayer resin insulating layer to form the multi-conductor circuit, and can be loaded IC Chip side surface, and can connect other side of the surface of the substrate to form welding projections, and in the substrate can be connected to the other side of the substrate surface and the other was between the resin sealing, characterized in that:

Will have access to the other side of the substrate surface welding protrusions formed in a plurality of interlayer hole.

中華民國專利公報 [19] [12]

[11]公告編號：398162
[44]中華民國 89年 (2000) 07月 11日
發明 全 15 頁

[51] Int.Cl [06]: H05K1/05

[54]名 稱：封裝基板

[21]申請案號： 087117123 [22]申請日期： 中華民國 87年 (1998) 10月 15日

[30]優 先 權：
[31]361947 [32]1997/12/10 [33]日本
[31]343815 [32]1997/11/28 [33]日本
[31]312687 [32]1997/10/29 [33]日本
[31]312686 [32]1997/10/29 [33]日本
[31]303694 [32]1997/10/17 [33]日本

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1 2

[57]申請專利範圍：

1.一種封裝基板，在核心基板的兩側隔著層間樹脂絕緣層形成有導體電路，且在可裝載IC晶片側的表面形成有焊接墊，並且在可連接其他基板側的表面形成有較上述IC晶片側所裝載之焊接墊相對大的焊接墊，其特徵在於：
在形成於上述核心基板可裝載IC晶片側的導體電路的圖案之間形成暫置圖案。

2.一種封裝基板，在核心基板的兩側隔著層間樹脂絕緣層形成有導體電路，且在可裝載IC晶片側的表面形成有焊接墊，並且在可連接其他基板側的表面形成有較上述IC晶片側所裝載之焊接墊相對大的焊接墊，其特徵在於：
在形成於上述核心基板可裝載IC晶片側的導體電路的圖案外周圍形成暫置圖案。

3.一種封裝基板，其為具備有最外層導體電路；支撐該最外層導體電路的絕緣層；以及設於該絕緣層下側的內層導體電路之多層線路板，其特徵在於：
上述內層導體電路為電源層及／或接地層，並且在穿透該絕緣層且連接該內層導體電路之介層孔上形成有一焊接凸出物。

4.一種封裝基板，其為具備有第1內層導體電路；形成於該第1層導體電路上方的第1層間樹脂絕緣層；形成於該第1層間樹脂絕緣層上方的第2內層導體電路；形成該該第2內層導體電路上方的第2層間樹脂絕緣層；及形成於該第2層間樹脂絕緣層上方的最外層導體電路之多層印刷線路板，其特徵在於：
上述第2內層導體電路為電源層及／或接地層，並且在穿透該第2層間樹脂絕緣層且連接該第2內層導體電路之介層孔上形成有一焊接凸出物。

3

5.一種封裝基板，在核心基板的兩面形成一導體層，並且再隔著層間樹脂絕緣層形成另一導體層，上述核心基板任一面的導體層可當作電極層使用，其特徵在於：

將裝配於當作上述電極層之導體層的核心基板穿透用通過孔的接地物；與用以連接穿透上面之層間樹脂絕緣層的介層孔之墊一體化。

6.一種封裝基板，在核心基板的兩面形成一導體層，並且再隔著層間樹脂絕緣層形成另一導體層，上述任一層間樹脂絕緣層上面的導體層可當作電極層使用，其特徵在於：

將裝配於當作上述電極層之導體層的下面層間樹脂絕緣層穿透用介層孔的接地物；與用以連接穿透上面之層間樹脂絕緣層的介層孔之墊一體化。

7.一種封裝基板，隔著複數個層間樹脂絕緣層形成有多層之導體電路，且可裝載IC晶片側的表面、及可連接其他基板側的表面形成有焊接凸出物，且在可連接該其他基板側的表面與該其他基板之間具有樹脂密封著，其特徵在於：

將可連接其他基板側的表面之焊接凸出物形成於介層孔上。

8.一種封裝基板，隔著複數個層間樹脂絕緣層形成有多層之導體電路，且可裝載IC晶片側的表面、及可連接其他基板側的表面形成有焊接凸出物，且在可連接該其他基板側的表面與該其他基板之間具有樹脂密封著，其特徵在於：

將可連接其他基板側的表面之焊接凸出物形成於複數個介層孔上。

圖式簡單說明：

第一圖顯示本發明第1實施例之封裝基板。

第二圖為第一圖所示之封裝基板的X1-X1橫剖面圖。

第三圖～第九圖為顯示本發明第1實施例之封裝基板的製程剖面圖。

4

第十圖顯示本發明第2實施例之封裝基板。

第十一圖(A)為第2實施例之封裝基板的上視圖。而第十一圖(B)為IC晶片的底面圖。

第十二圖顯示將IC晶片裝載於第十圖所示的封裝基板，並且安裝於母板的狀態。

第十三圖顯示本發明第3實施例之多層印刷線路板之剖面圖。

第十四圖顯示本發明第3實施例之變更例多層印刷線路板之剖面圖。

第十五圖顯示本發明第4實施例之封裝基板剖面圖。

第十六圖(A)為第4實施例的內層銅圖案之形成核心基板上視圖。第十六圖(B)為第十六圖(A)的一部分放大圖。

第十七圖顯示本發明第4實施例變更例封裝基板之剖面圖。

第十八圖(A)為形成於第4實施例變更例之封裝基板的導體電路上視圖。第十八圖(B)為第十八圖(A)的一部分放大圖。

第十九圖顯示本發明第5實施例之封裝基板的剖面圖。

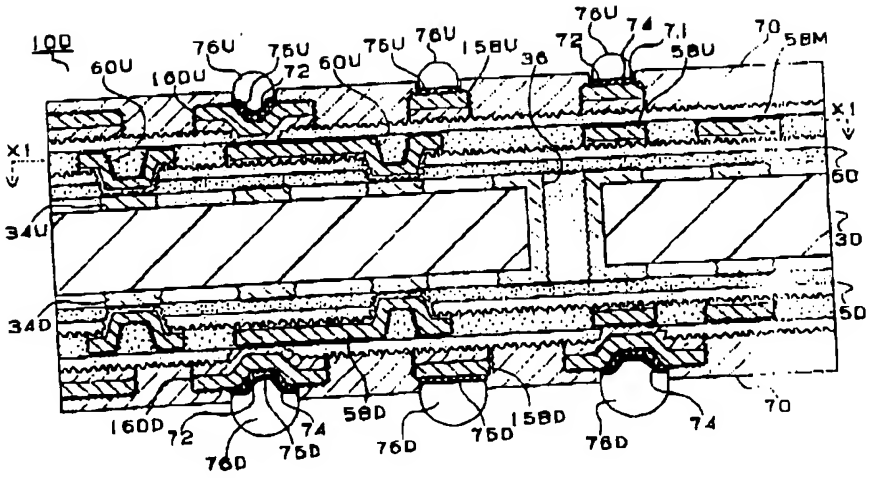
第二十圖顯示將IC晶片裝載於第十九圖所示的封裝基板，並且安裝於母板的狀態。

第二十一圖為本發明第5實施例之變更例封裝基板之剖面圖。

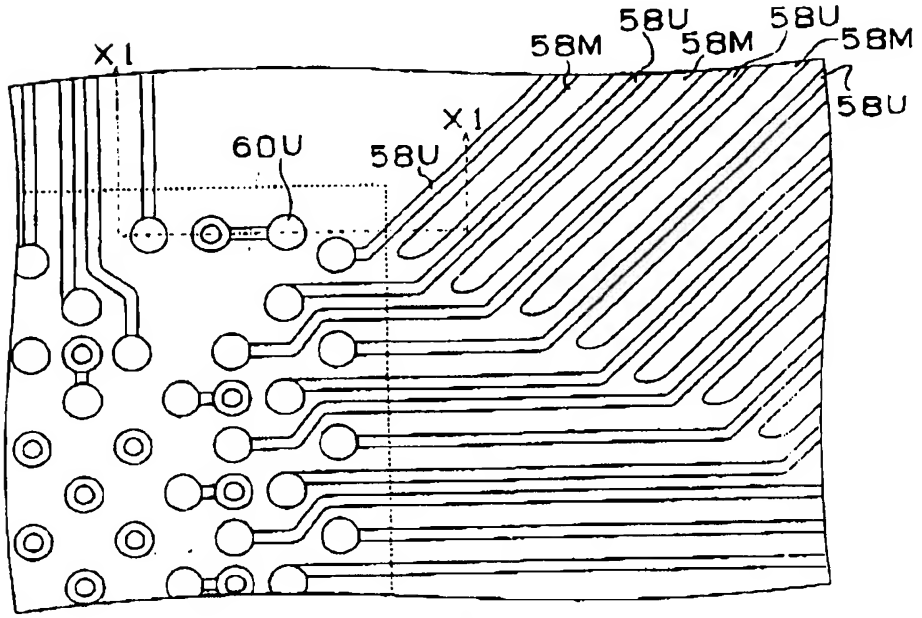
第二十二圖為第二十一圖之X5-X5之橫剖面圖。

第二十三圖為習知技術之封裝基板剖面圖。

第二十四圖(A)為第二十三圖之內層導體電路的上視圖。第二十四圖(B)為第二十三圖之C箭頭方向觀看圖。第二十四圖(C)為第二十三圖之D箭頭方向觀看圖。

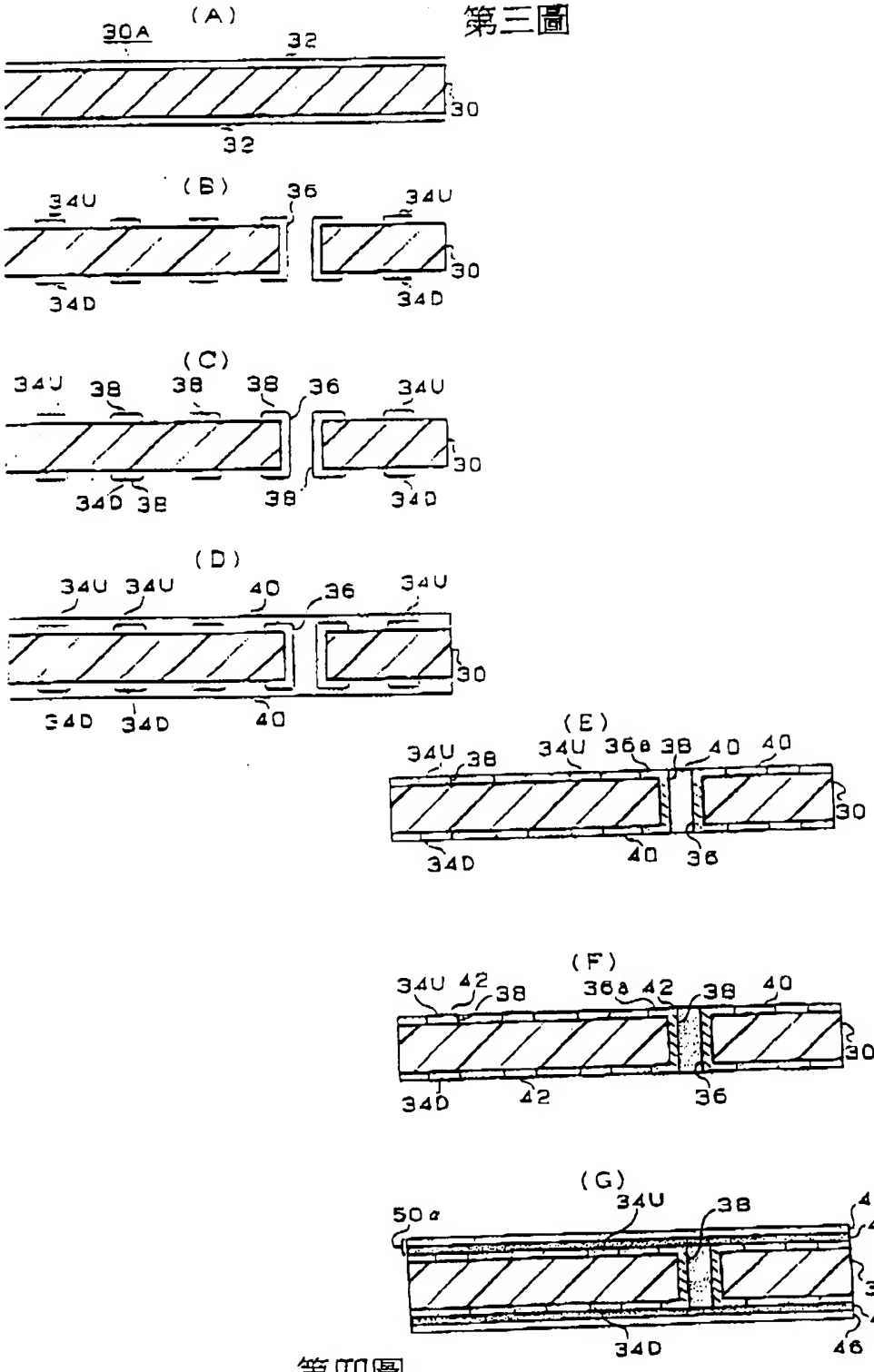


第一圖



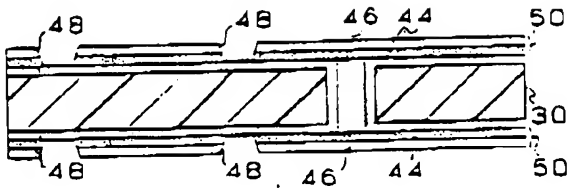
第二圖

第三圖



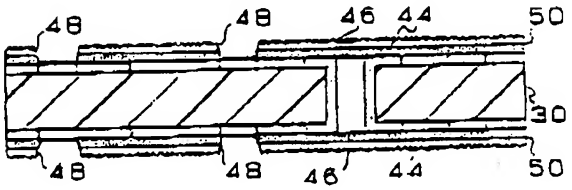
第四圖

(H)

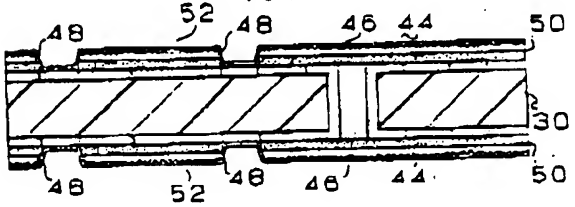


第五圖

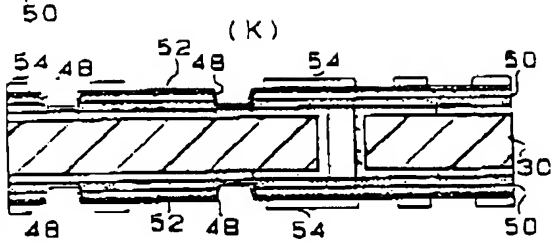
(I)



(J)



(K)



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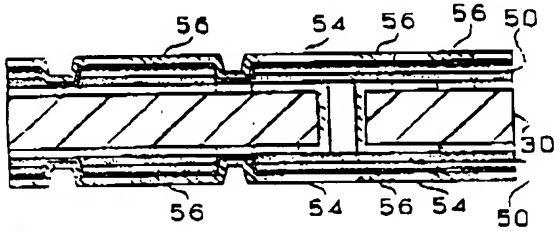
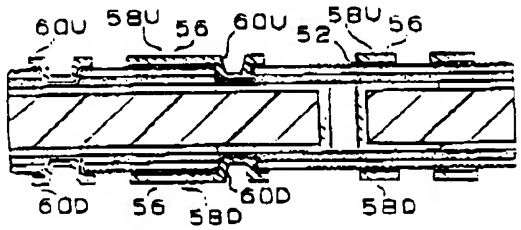
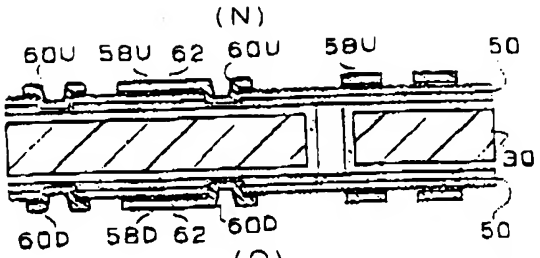
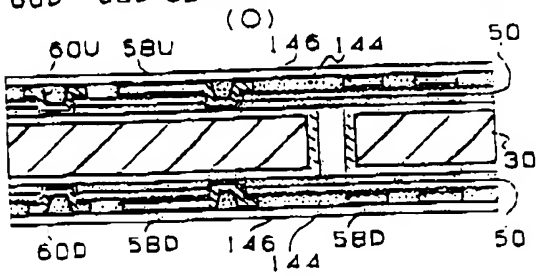


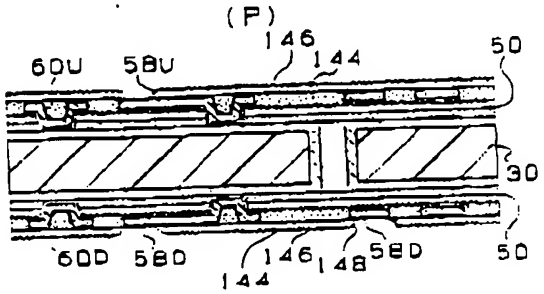
第六圖

(M)









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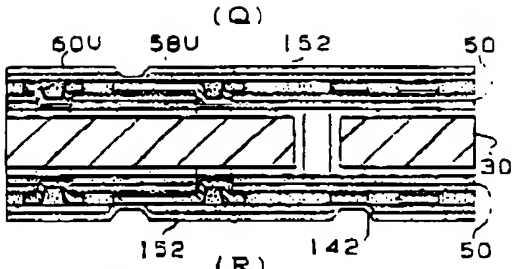
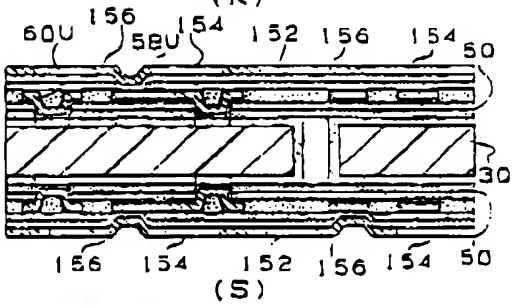
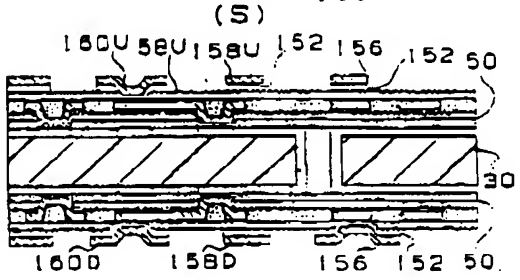
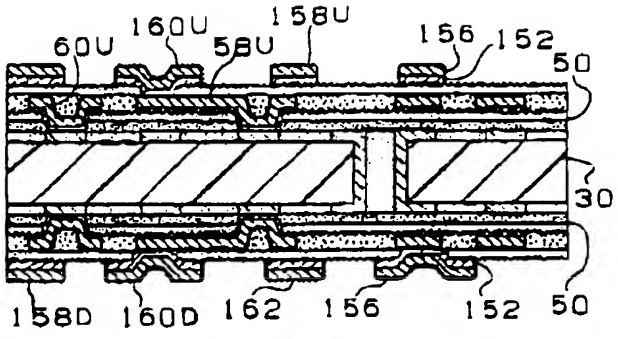




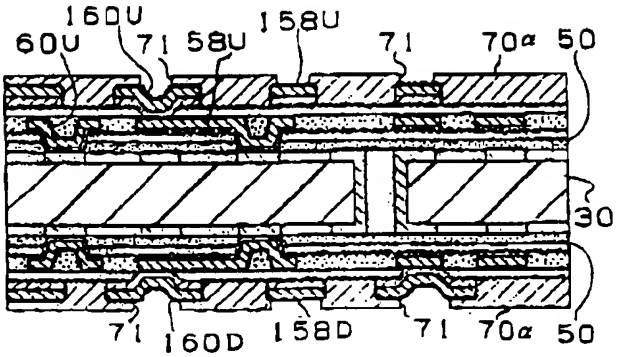


第八圖

(T)

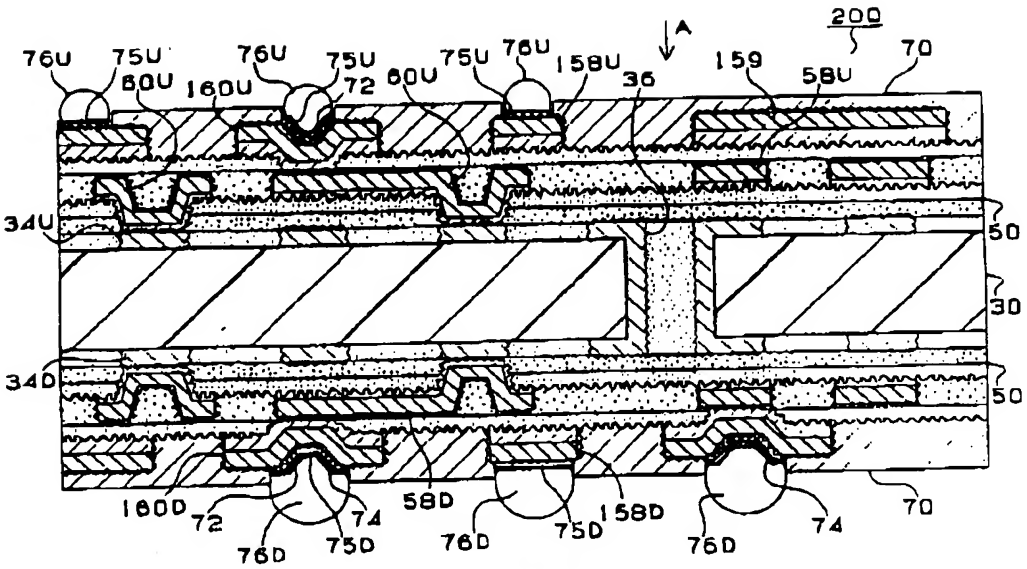


(U)

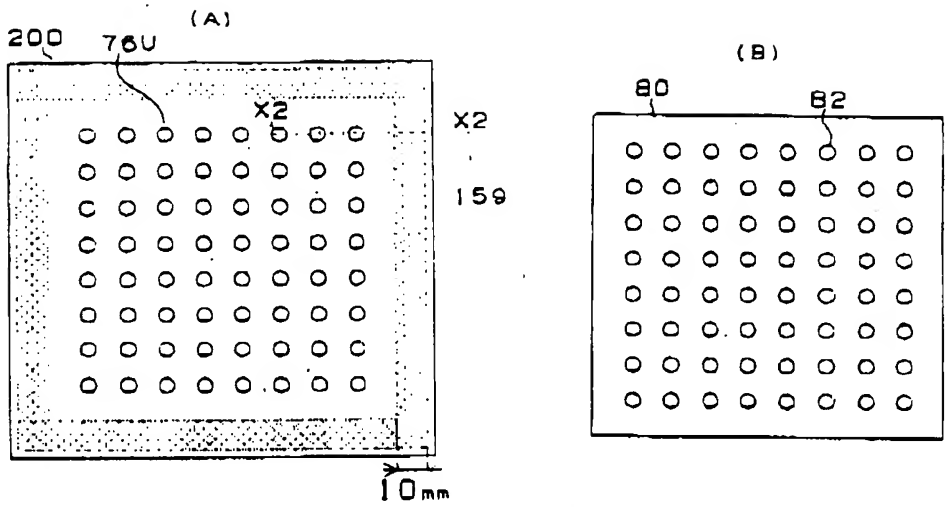


第九圖

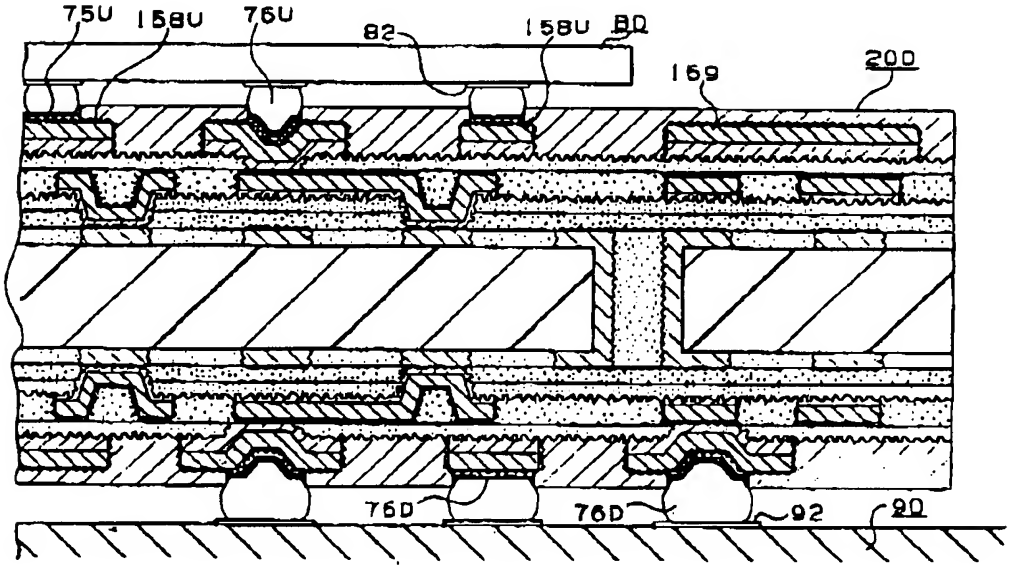
(8)



第十圖



第十一圖



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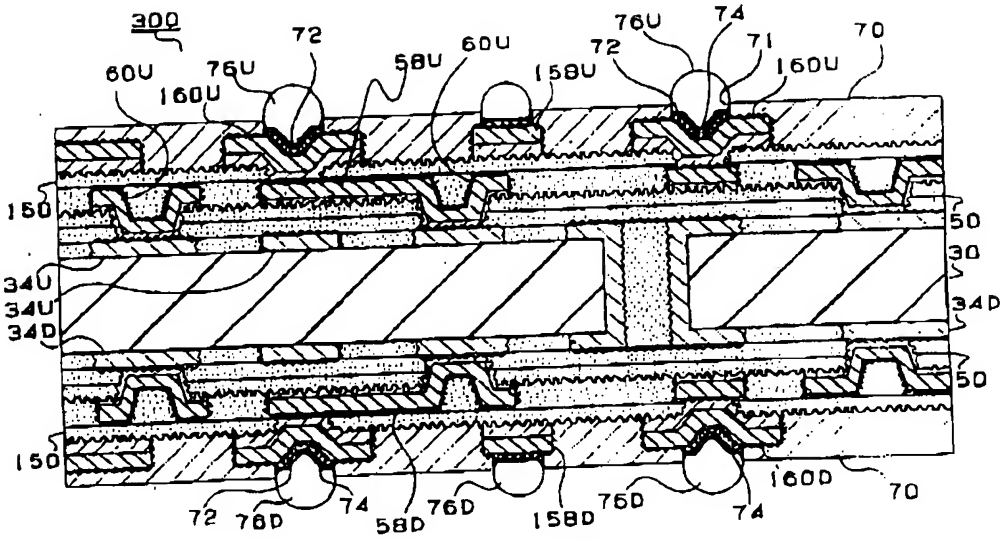

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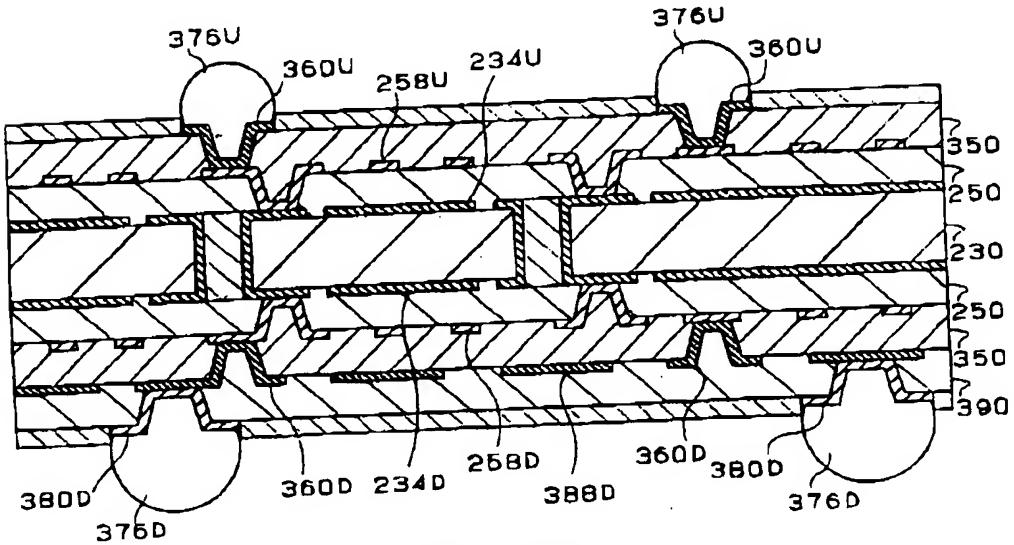

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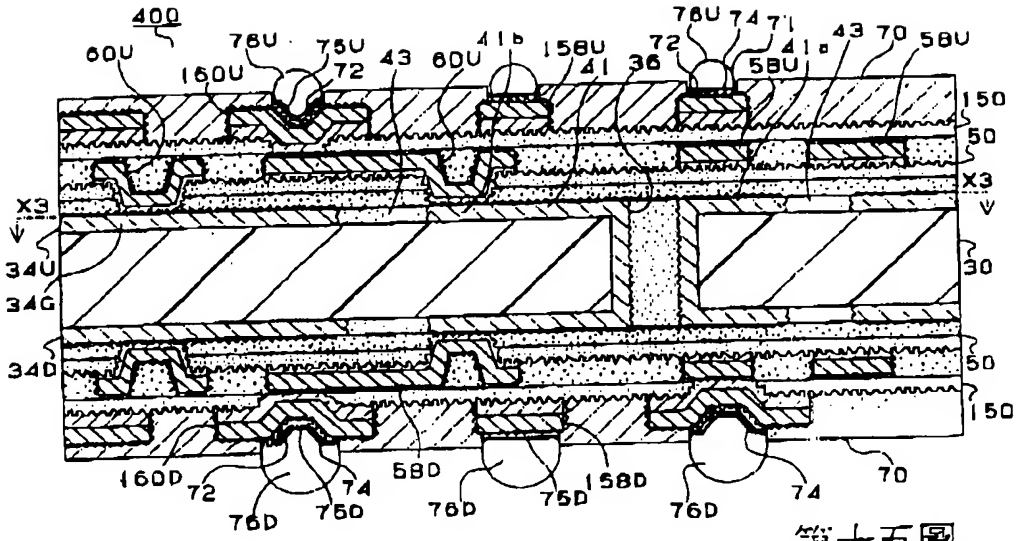

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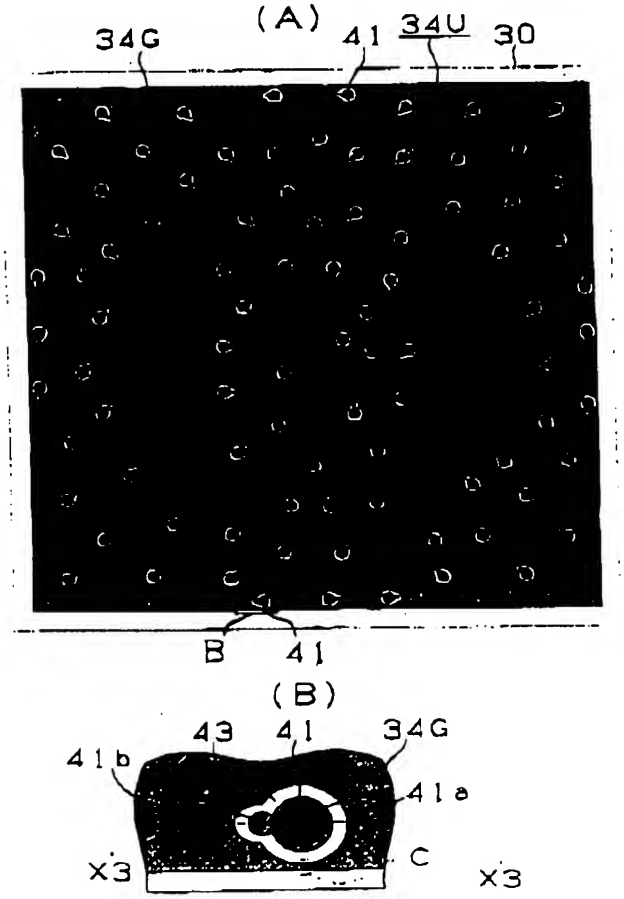

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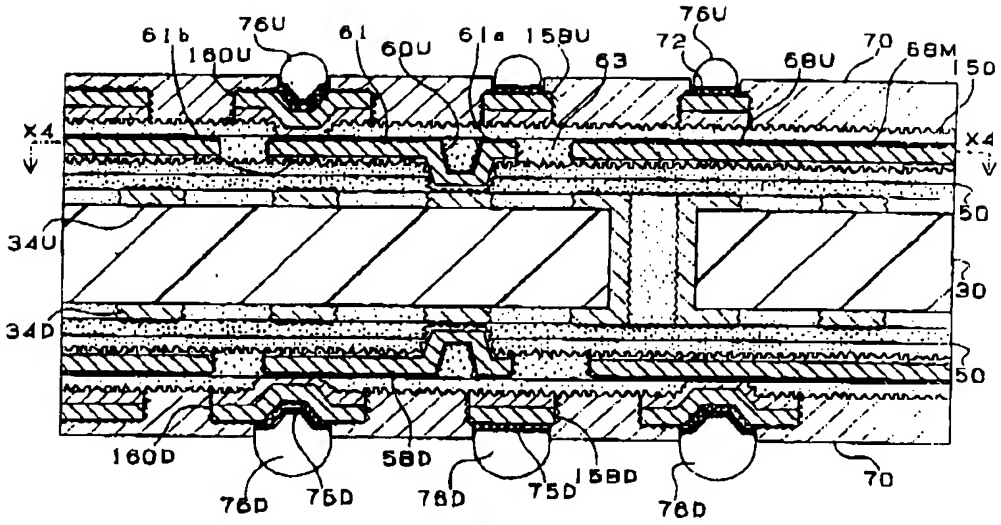

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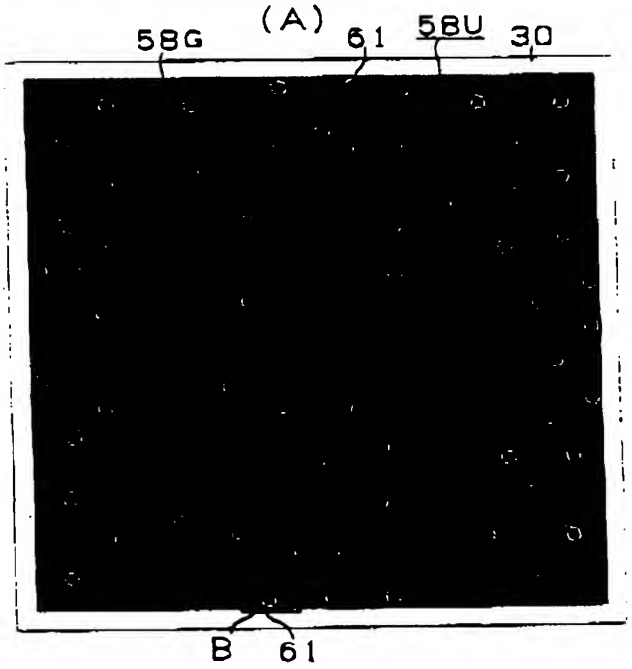

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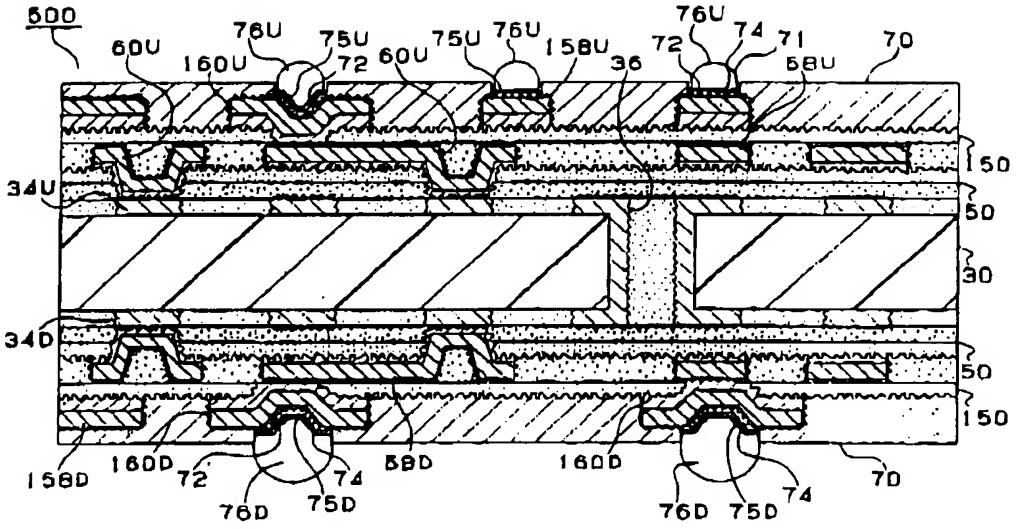

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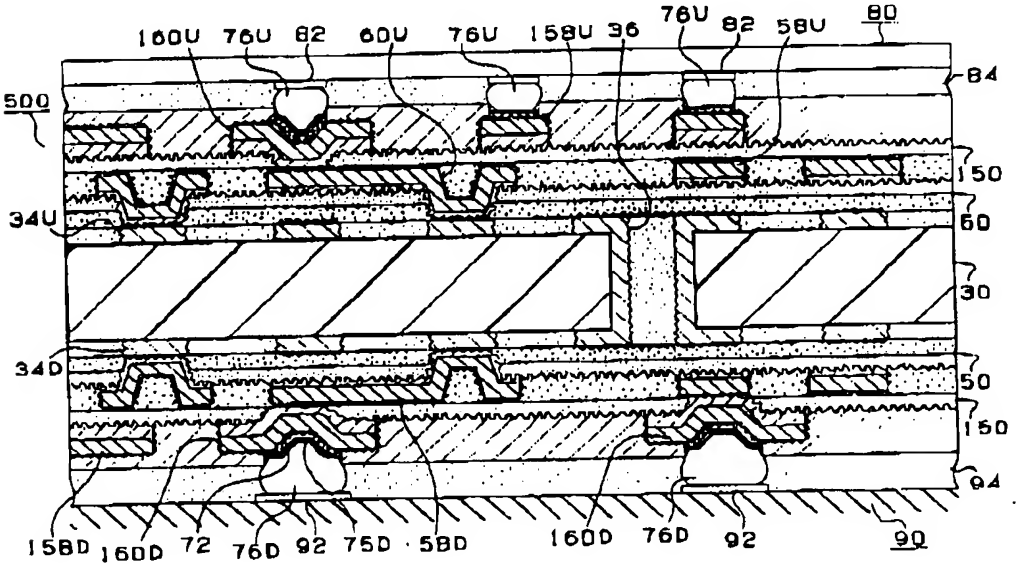

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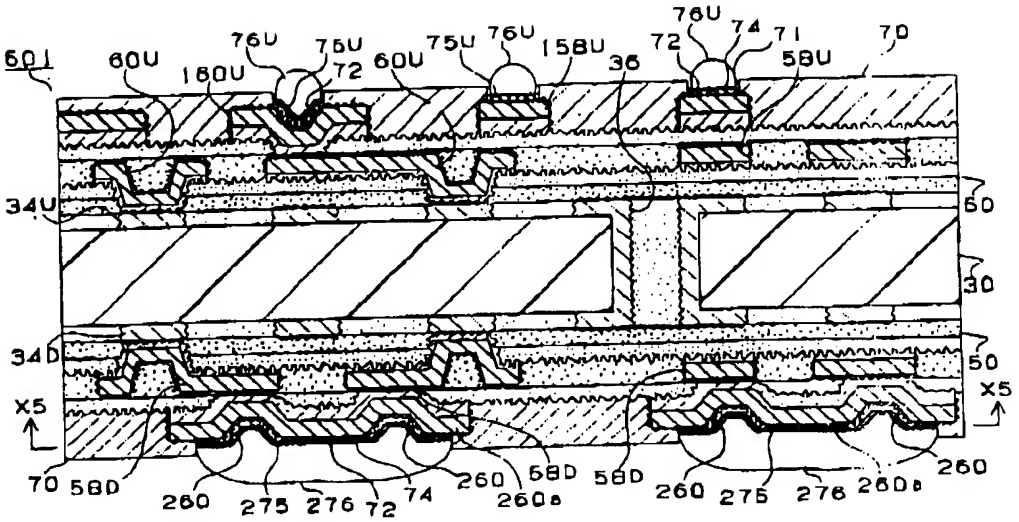

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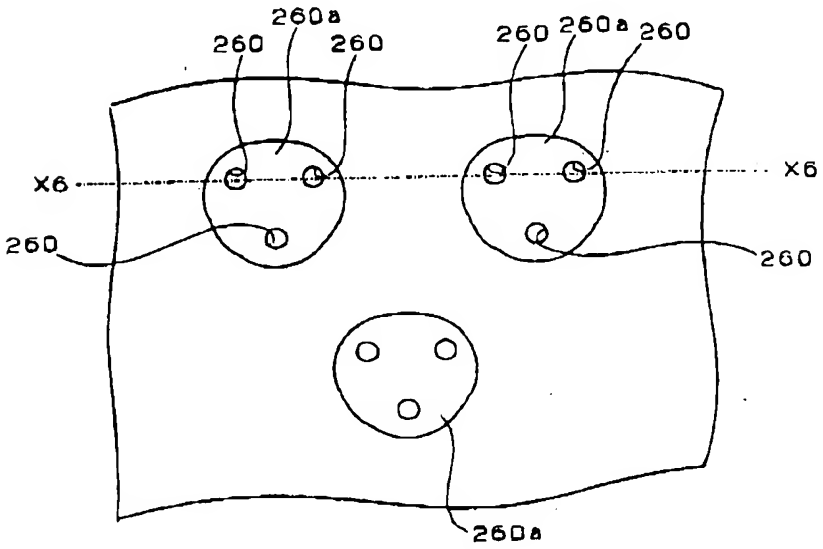

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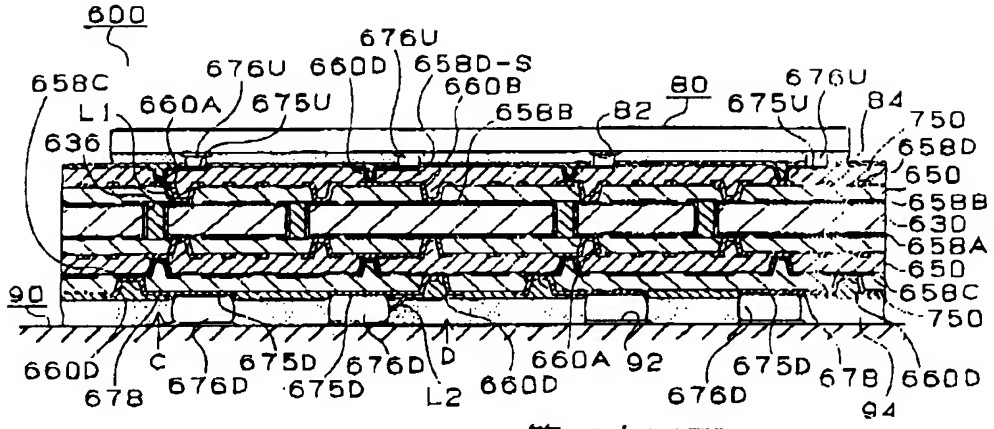

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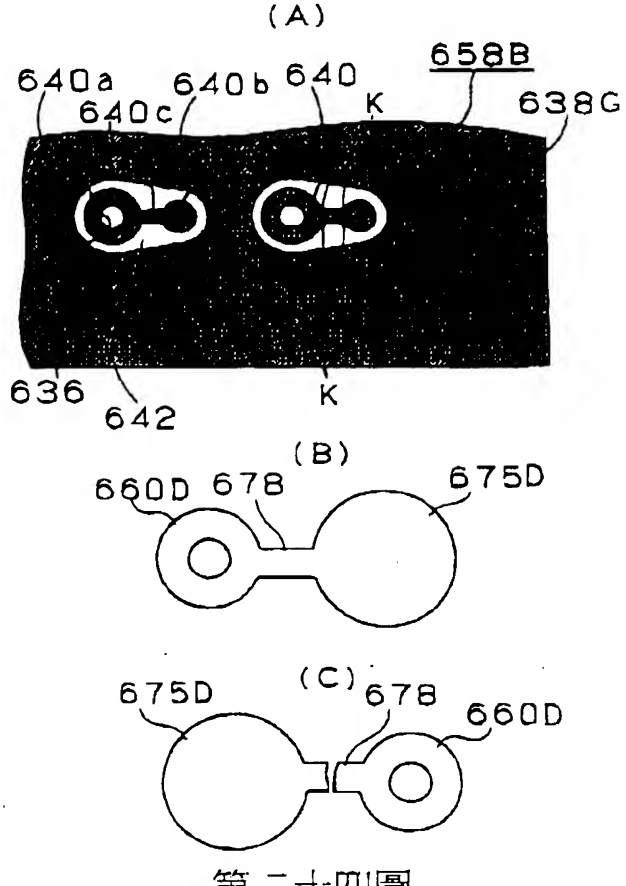

第二十四圖